FIG. 1

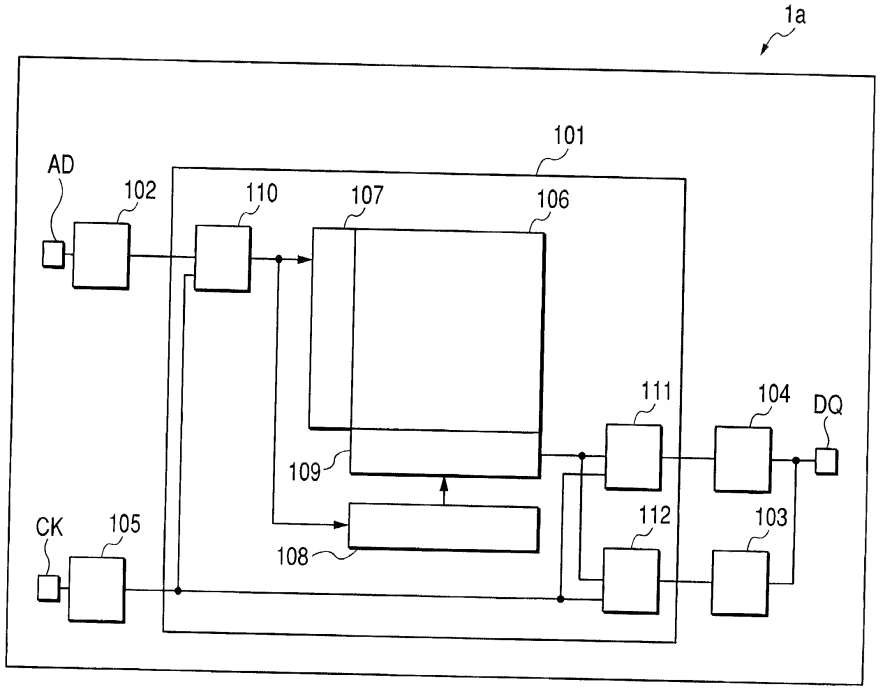


FIG. 2

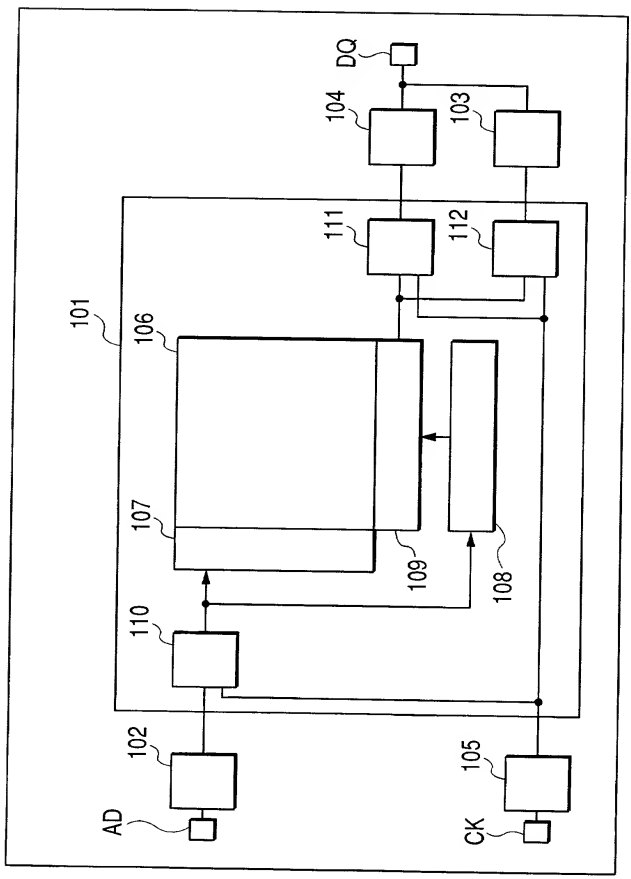


FIG. 3

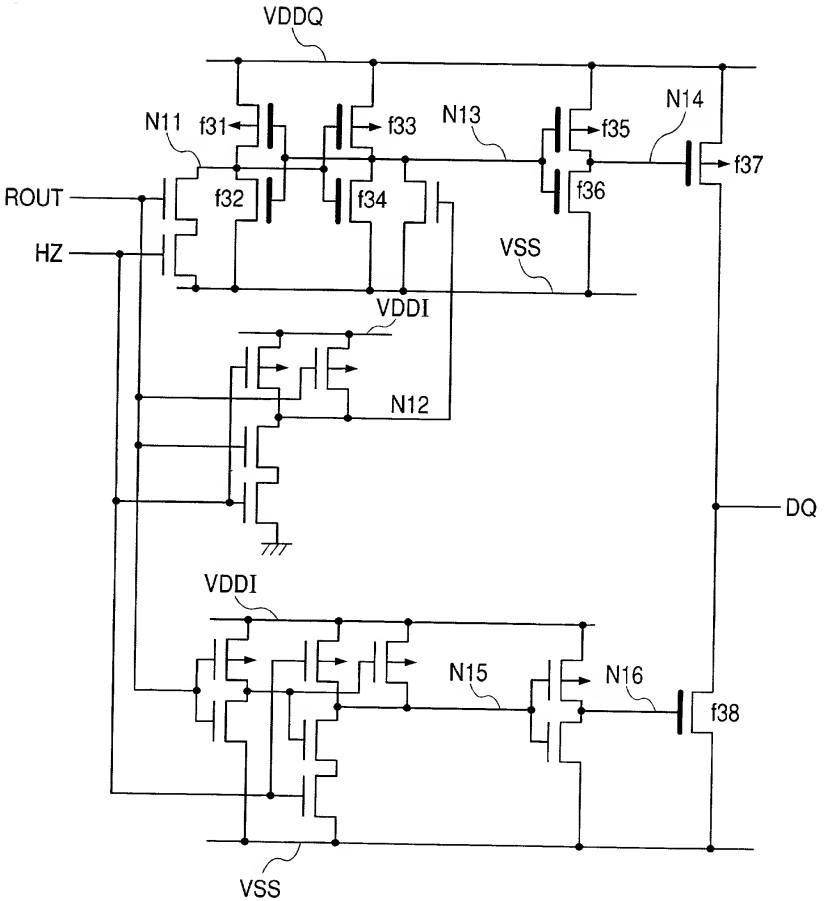

VDDQ
N11
f31
f33
N13
f35
N14
f37
ROUT
f32
f34
f36
HZ
VSS
VDDI
N12
DQ
VDDI
N15
N16
f38
VSS

FIG. 4

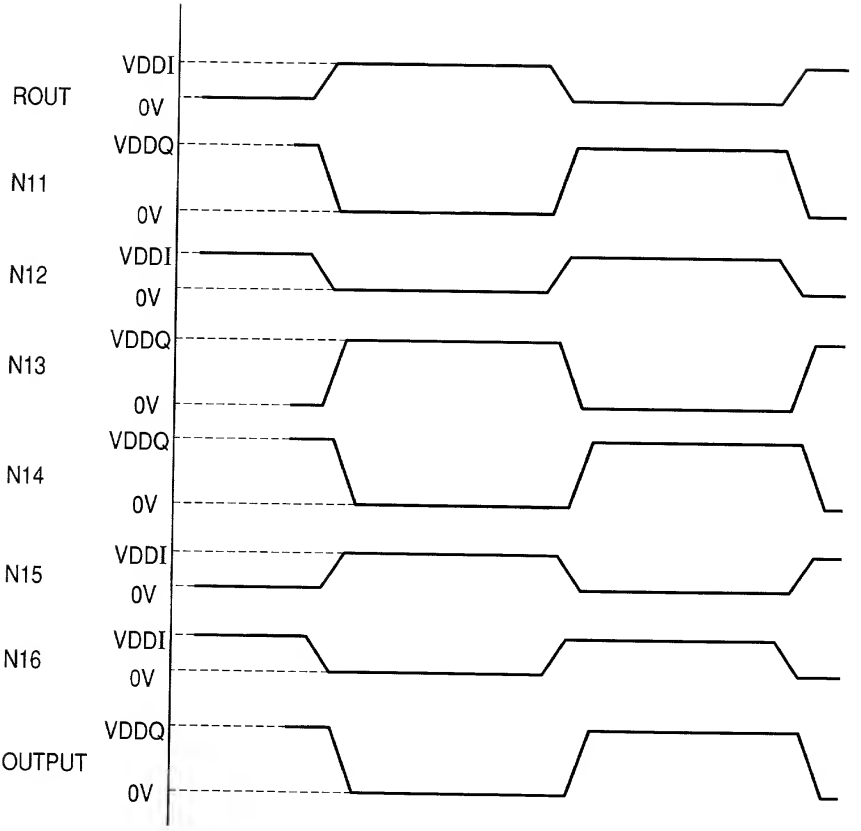

ROUT
VDDI
0V
N11
VDDQ
0V
N12
VDDI
0V
N13
VDDQ
0V
N14
VDDQ
0V
N15
VDDI
0V
N16
VDDI
0V
OUTPUT
VDDQ
0V

FIG. 5

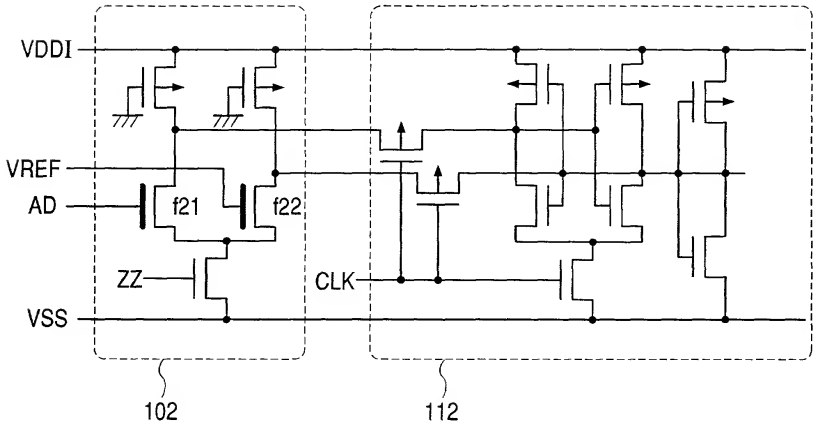

VDDI
VREF
AD
f21
f22
ZZ
CLK
VSS
102
112

FIG. 6

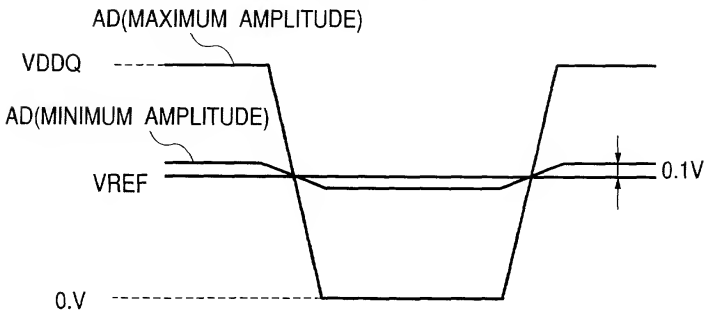
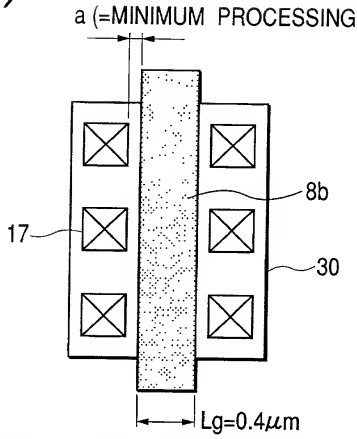
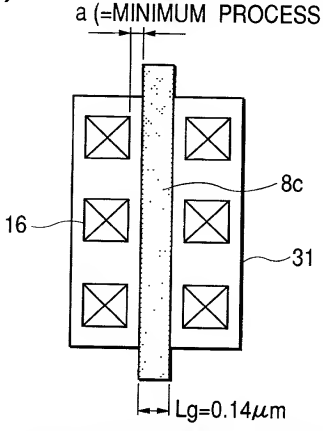

AD(MAXIMUM AMPLITUDE)
VDDQ
AD(MINIMUM AMPLITUDE)
VREF
0.1V
0.V

FIG. 7(a)



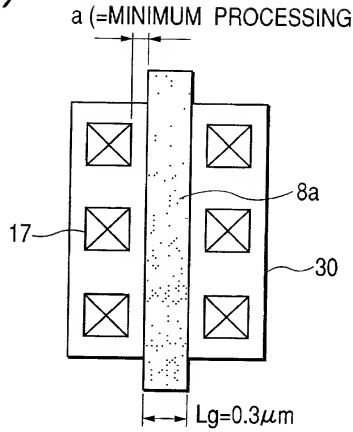
3.3V WITHSTANDING MOS TRANSISTOR

FIG. 7(b)



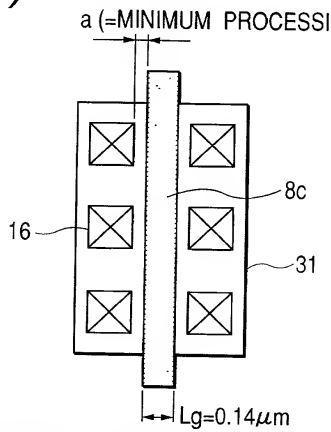
1.5V WITHSTANDING MOS TRANSISTOR

FIG. 8(a)



2.5V WITHSTANDING MOS TRANSISTOR

FIG. 8(b)



1.5V WITHSTANDING MOS TRANSISTOR

FIG. 9

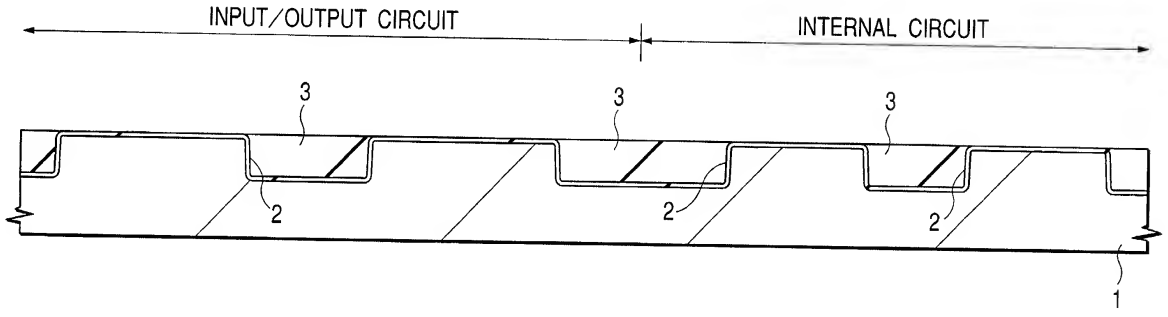

INPUT/OUTPUT CIRCUIT
INTERNAL CIRCUIT
3
3
3
2
2
2
1

FIG. 10

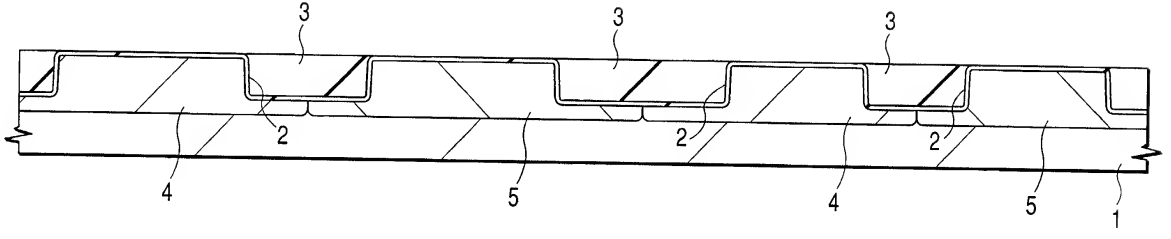

3
3
3
2
2
2
4
5
4
5
1

FIG. 11(a)

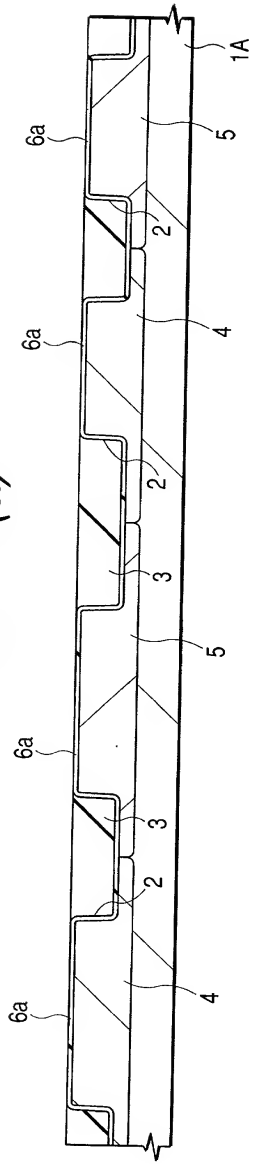


FIG. 11(b)

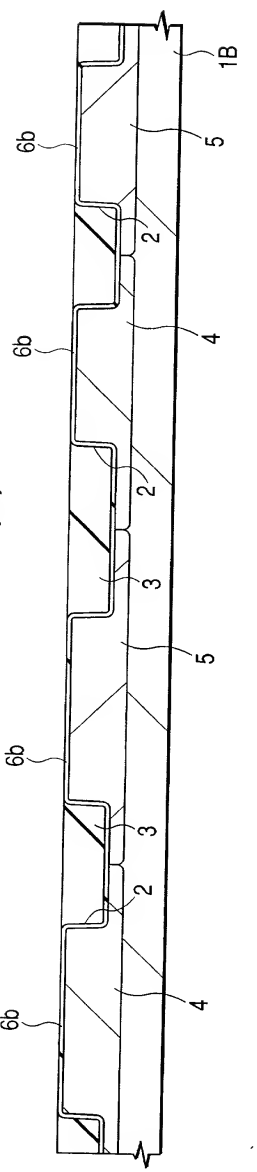


FIG. 12(a)

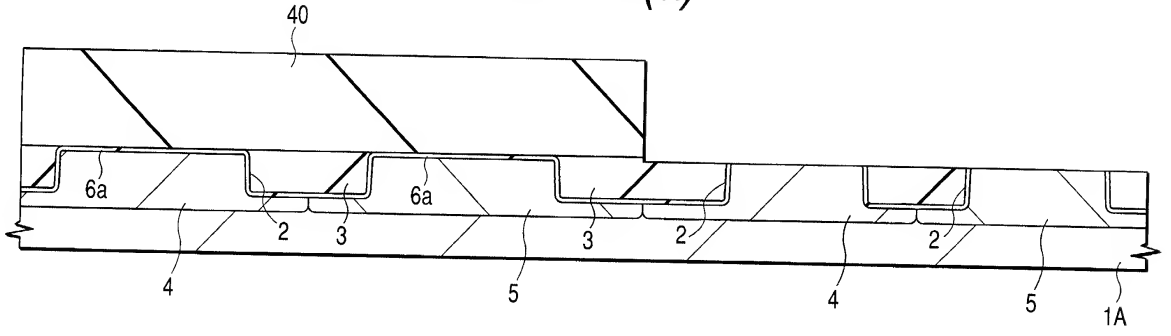


FIG. 12(b)

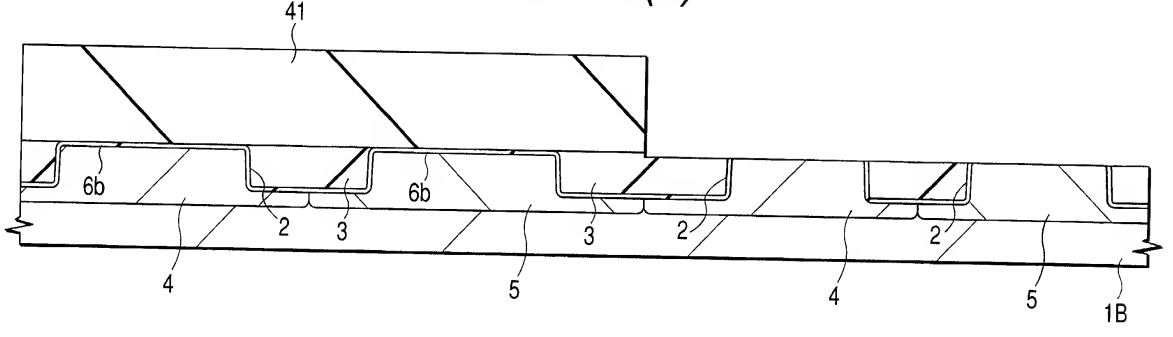


FIG. 13(a)

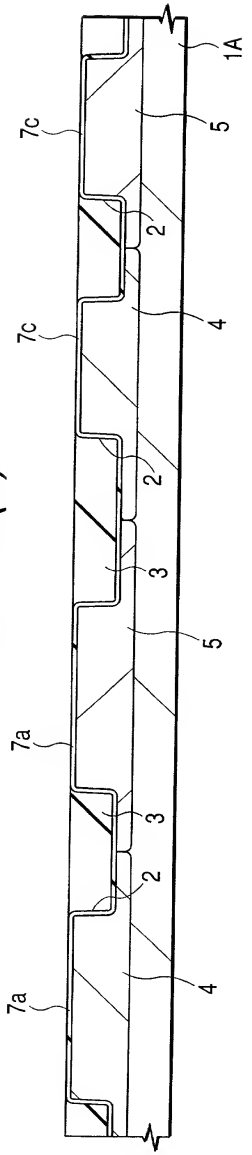


FIG. 13(b)

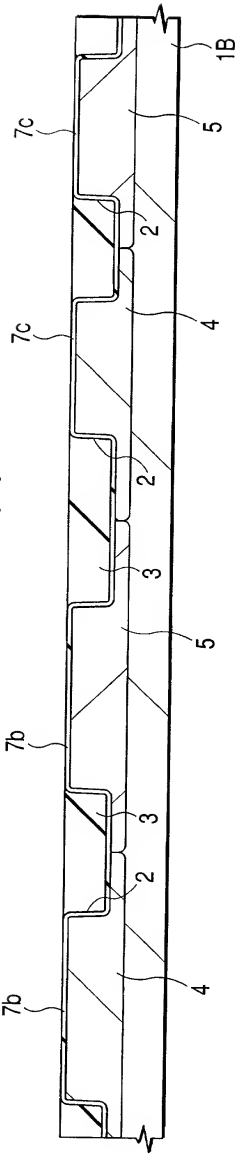


FIG. 14(a)

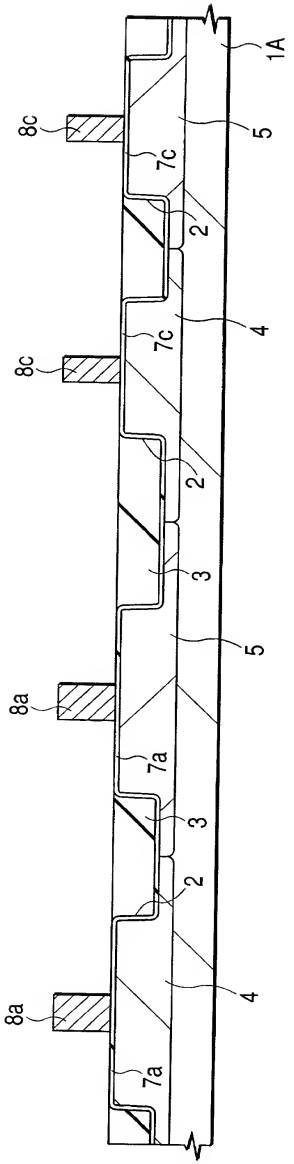


FIG. 14(b)

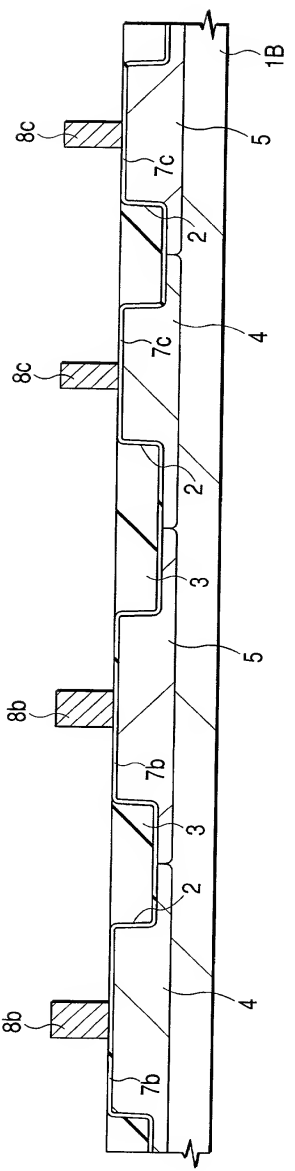


FIG. 15(a)

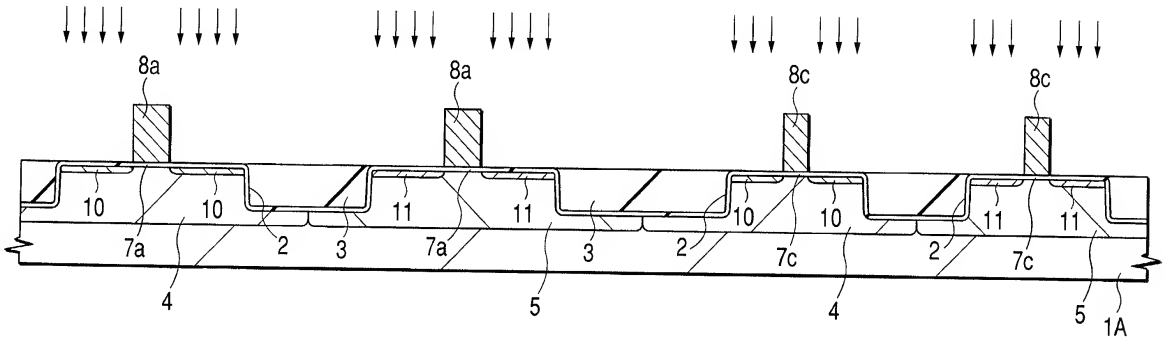


FIG. 15(b)

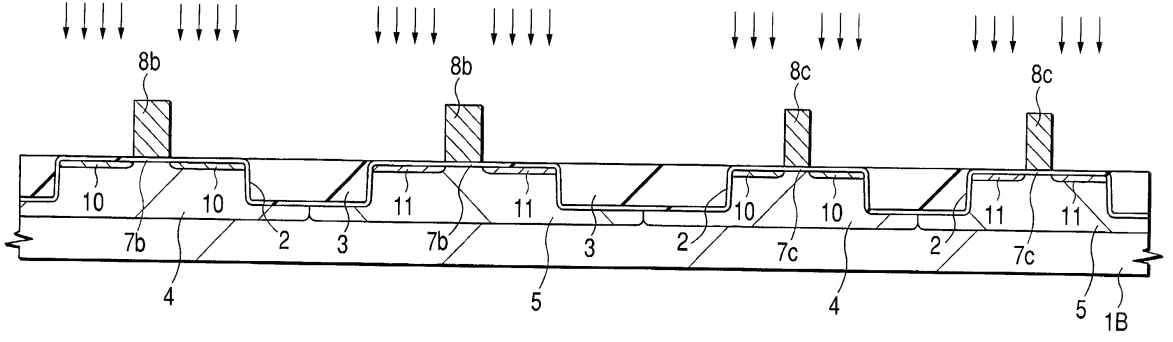


FIG. 16(a)

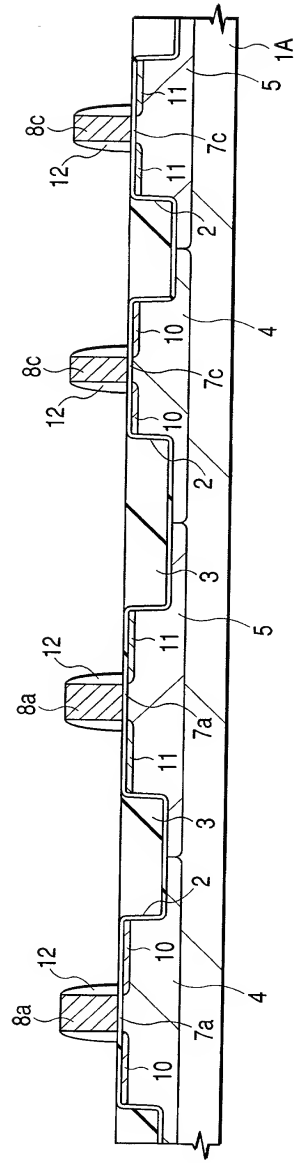


FIG. 16(b)

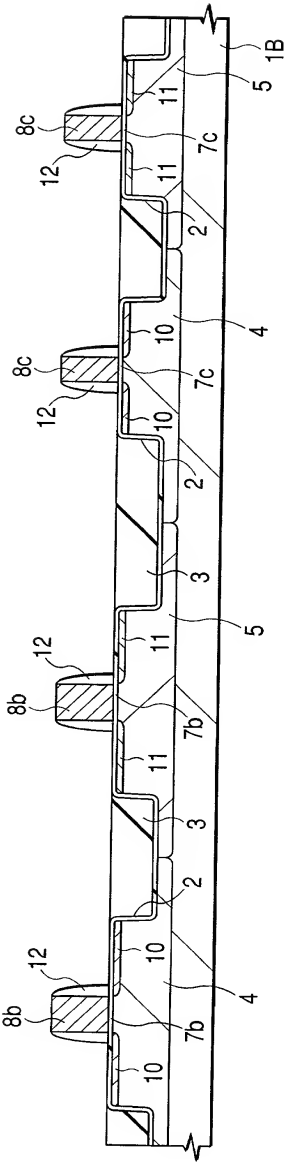


FIG. 17(a)

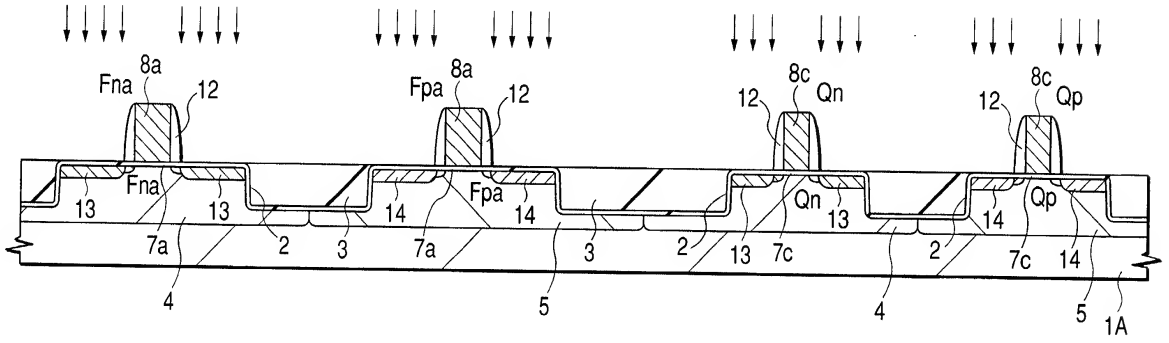


FIG. 17(b)

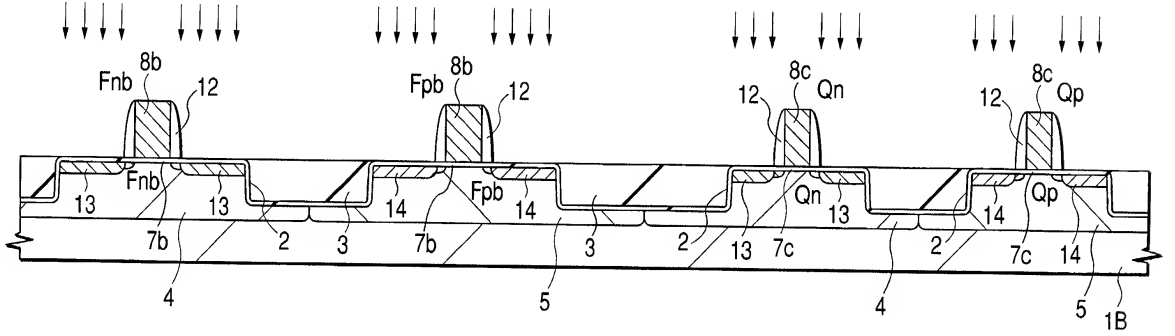


FIG. 18(a)

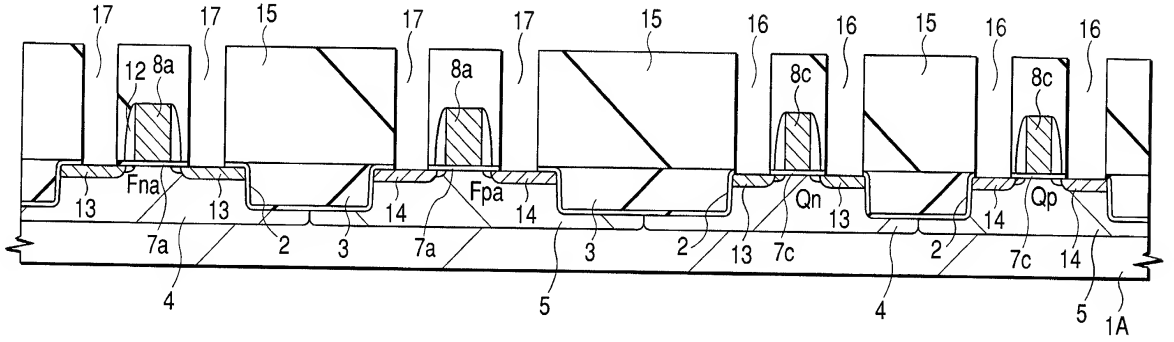


FIG. 18(b)

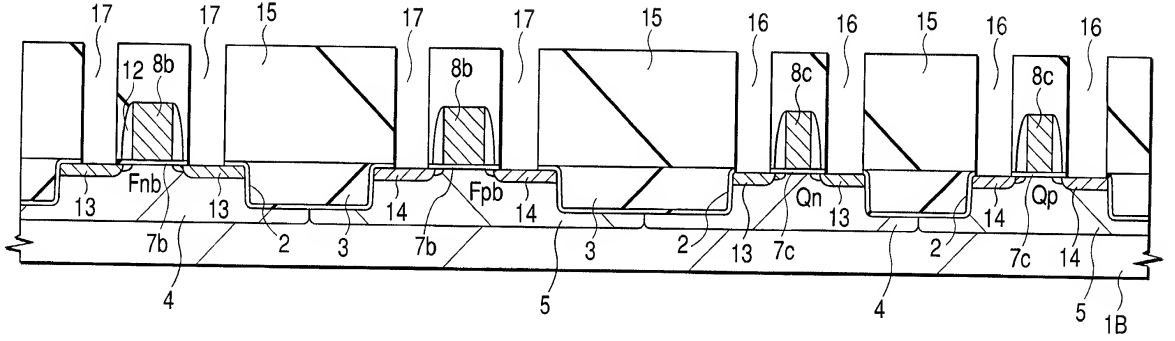


FIG. 19

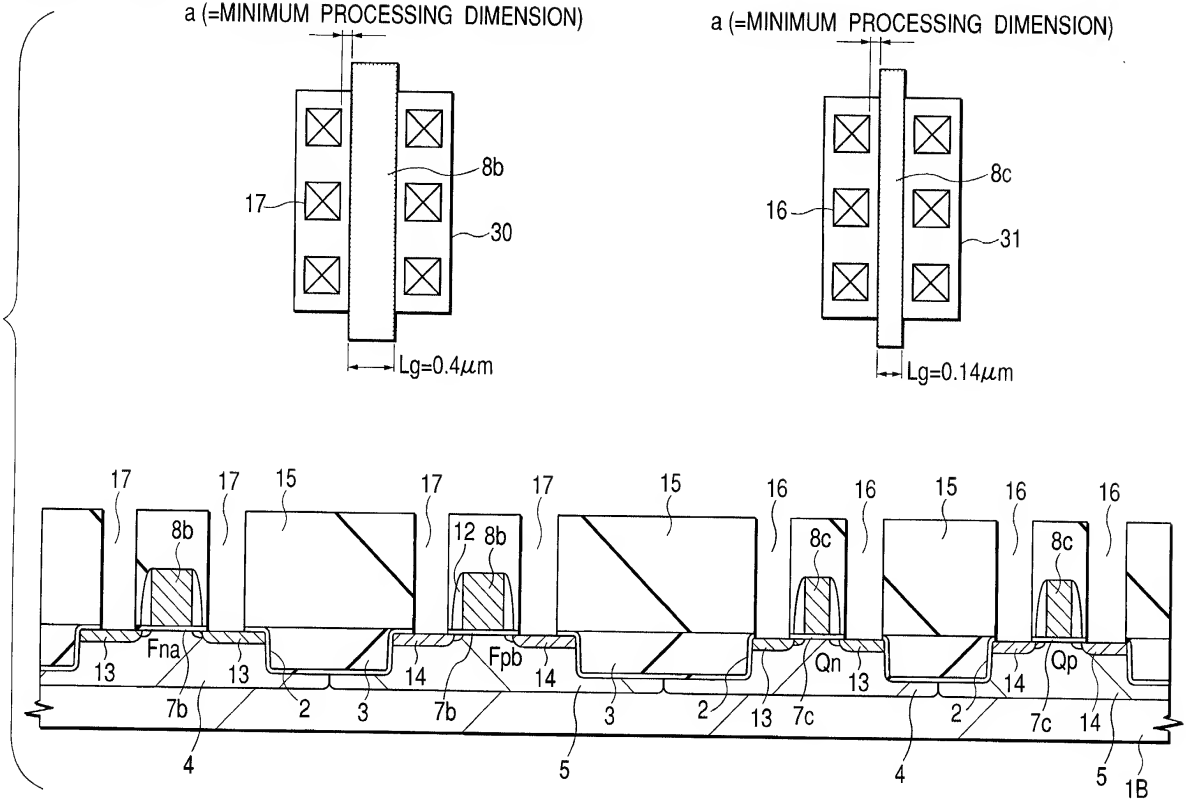

a (=MINIMUM PROCESSING DIMENSION)
8b
17
30
Lg=0.4μm
a (=MINIMUM PROCESSING DIMENSION)
8c
16
31
Lg=0.14μm
17
15
12
16
Fna
Fpb
Qn
Qp
13
14
7b
7c
2
3
4
5
1B

FIG. 20

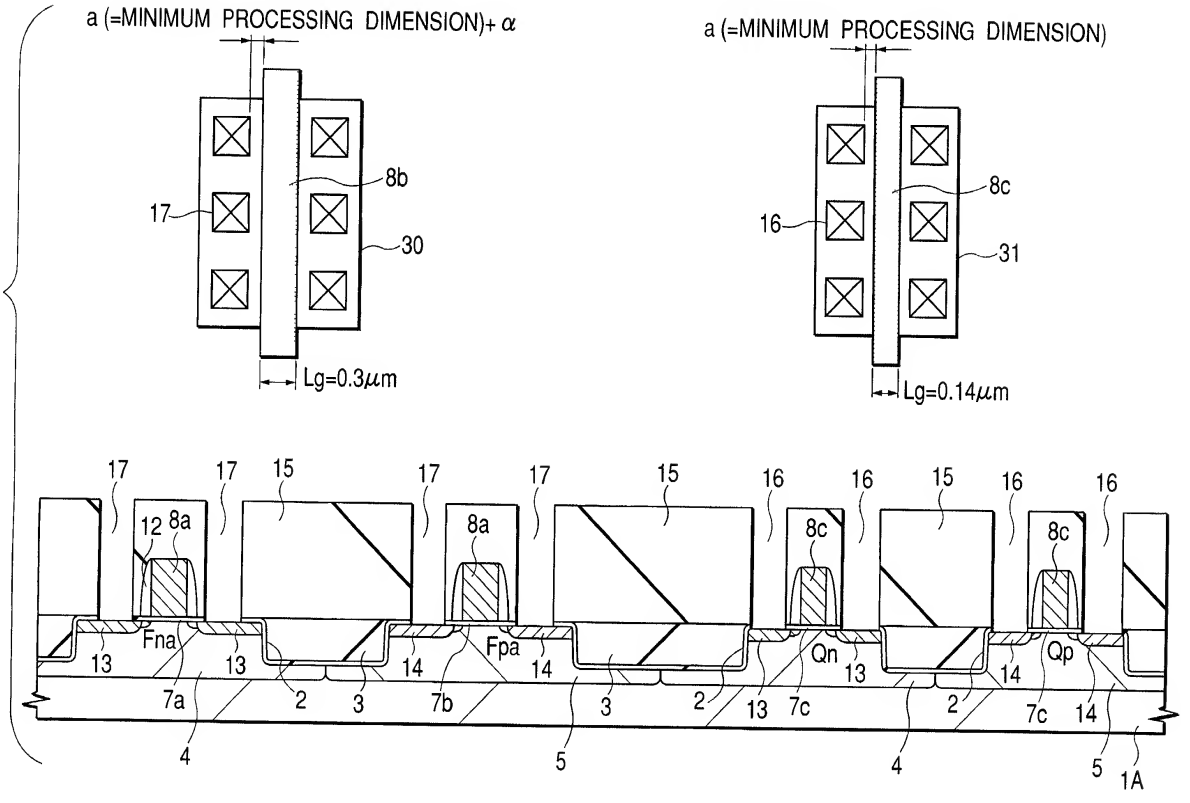

a (=MINIMUM PROCESSING DIMENSION)+ α
8b
17
30
Lg=0.3μm
a (=MINIMUM PROCESSING DIMENSION)
8c
16
31
Lg=0.14μm
17
12
8a
15
Fna
Fpa
Qn
Qp
13
14
7a
7b
7c
2
3
4
5
1A

FIG. 21

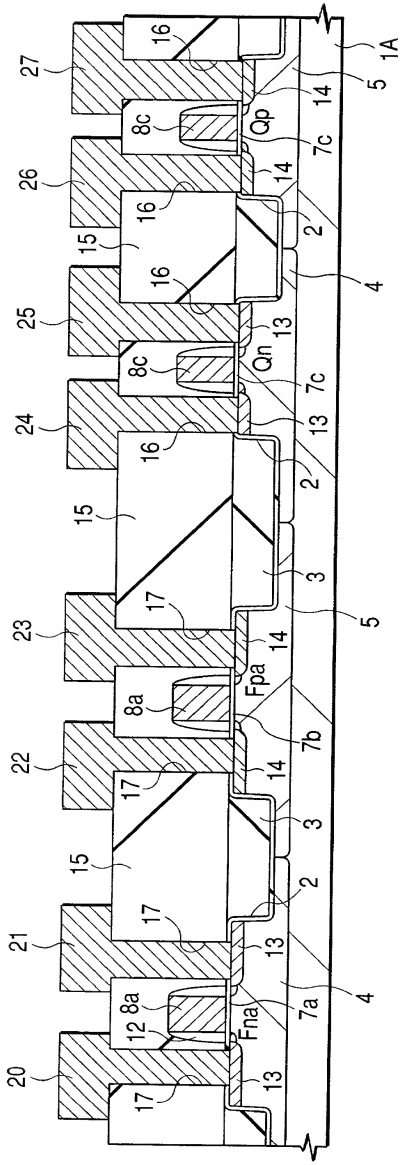

1A
2
3
4
5
7a
7b
7c
8a
8c
12
13
14
15
16
17
20
21
22
23
24
25
26
27
Fna
Fpa
Qn
Qp

FIG. 22

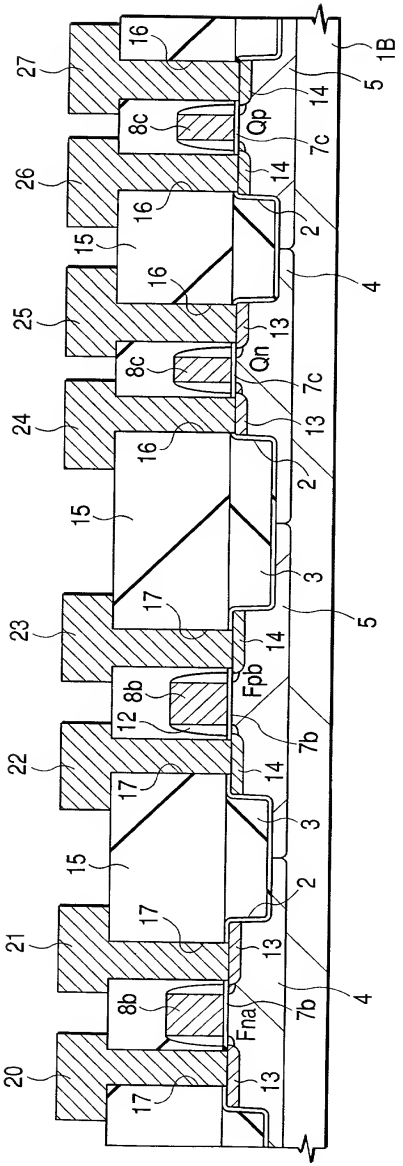

1B
5
14
Qp
7c
14
2
4
Qn
13
7c
13
2
3
5
14
Fpb
8b
12
7b
14
3
2
13
4
7b
Fna
13
16
8c
16
16
8c
16
17
17
17
17
8b
8b
15
15
15
20
21
22
23
24
25
26
27

FIG. 23

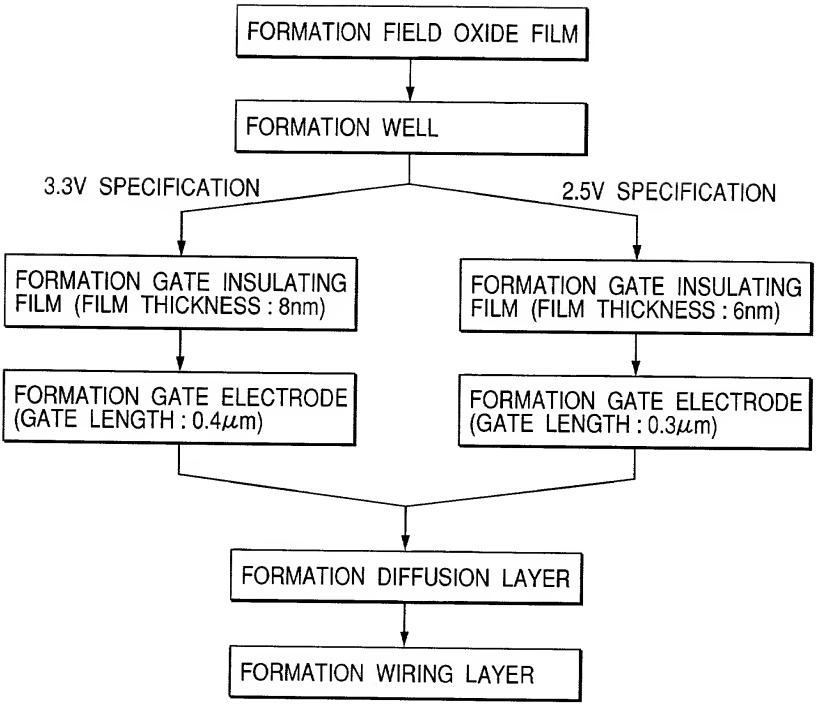

FORMATION FIELD OXIDE FILM
FORMATION WELL
3.3V SPECIFICATION
2.5V SPECIFICATION
FORMATION GATE INSULATING FILM (FILM THICKNESS : 8nm)
FORMATION GATE INSULATING FILM (FILM THICKNESS : 6nm)
FORMATION GATE ELECTRODE (GATE LENGTH : 0.4μm)
FORMATION GATE ELECTRODE (GATE LENGTH : 0.3μm)
FORMATION DIFFUSION LAYER
FORMATION WIRING LAYER

FIG. 24

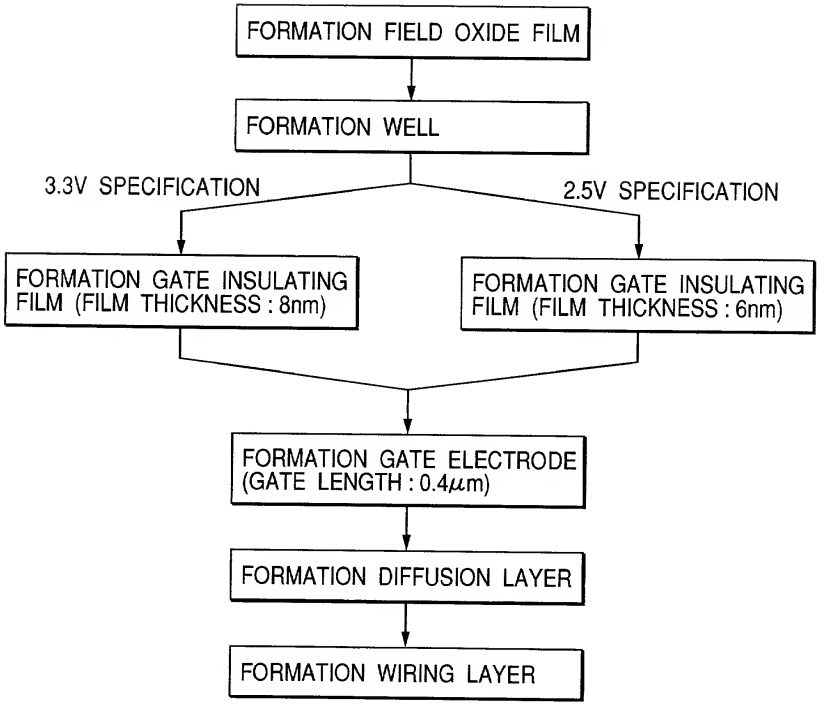

FORMATION FIELD OXIDE FILM
FORMATION WELL
3.3V SPECIFICATION
2.5V SPECIFICATION
FORMATION GATE INSULATING FILM (FILM THICKNESS : 8nm)
FORMATION GATE INSULATING FILM (FILM THICKNESS : 6nm)
FORMATION GATE ELECTRODE (GATE LENGTH : 0.4μm)
FORMATION DIFFUSION LAYER
FORMATION WIRING LAYER

FIG. 25

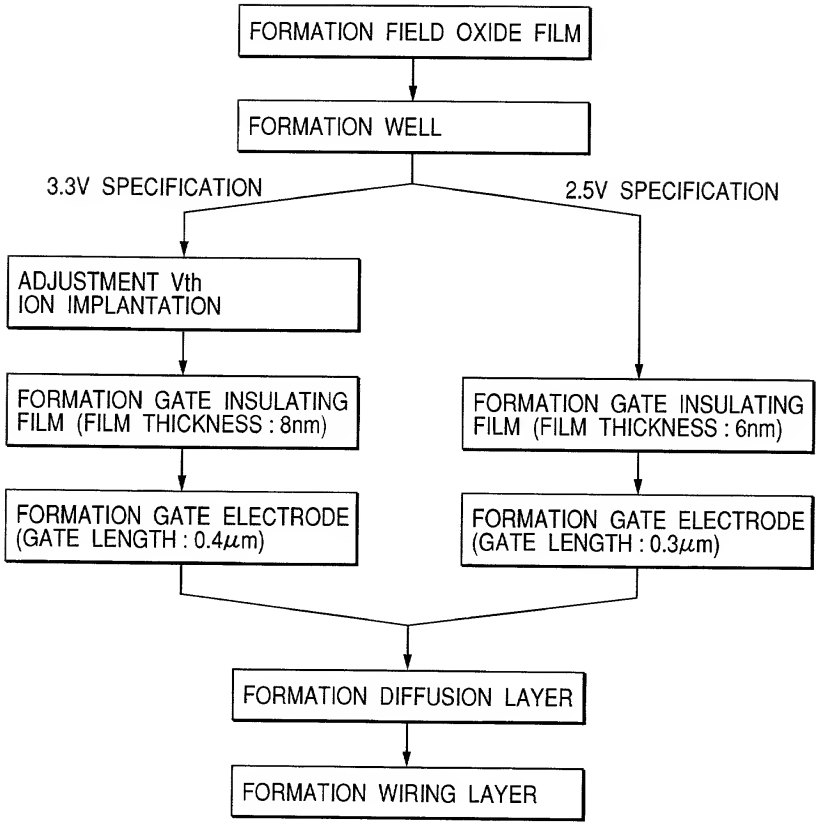
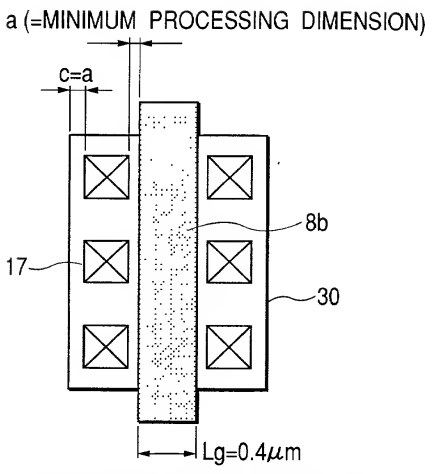
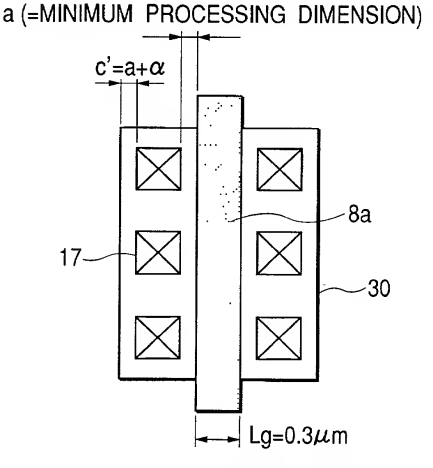

FORMATION FIELD OXIDE FILM
FORMATION WELL
3.3V SPECIFICATION
2.5V SPECIFICATION
ADJUSTMENT Vth
ION IMPLANTATION
FORMATION GATE INSULATING FILM (FILM THICKNESS : 8nm)
FORMATION GATE INSULATING FILM (FILM THICKNESS : 6nm)
FORMATION GATE ELECTRODE (GATE LENGTH : 0.4μm)
FORMATION GATE ELECTRODE (GATE LENGTH : 0.3μm)
FORMATION DIFFUSION LAYER
FORMATION WIRING LAYER

FIG. 26



3.3V WITHSTANDING MOS TRANSISTOR

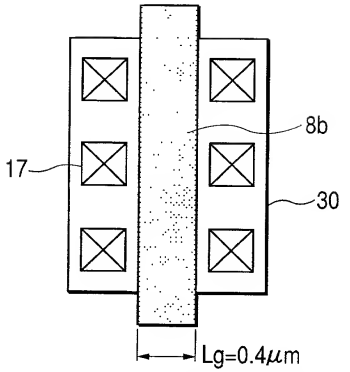


2.5V WITHSTANDING MOS TRANSISTOR

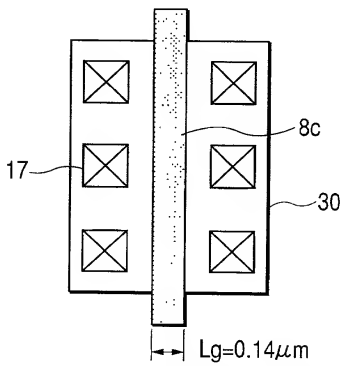
FIG. 27

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	1.5V	0V	VDDQ	1.5V

FIG. 28



3.3V WITHSTANDING MOS TRANSISTOR



2.5V WITHSTANDING MOS TRANSISTOR

FIG. 29

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	2.5V	0V	VDDQ	1.5V

FIG. 30

	GATE INSULATING FILM THICKNESS	MINIMUM PROCESSING GATE LENGTH
	TOX	Lg
3.3V WITHSTANDING MOS	8nm	0.4μm
2.5V WITHSTANDING MOS	6nm	0.3μm
1.5V WITHSTANDING MOS	3nm	0.14μm

FIG. 31

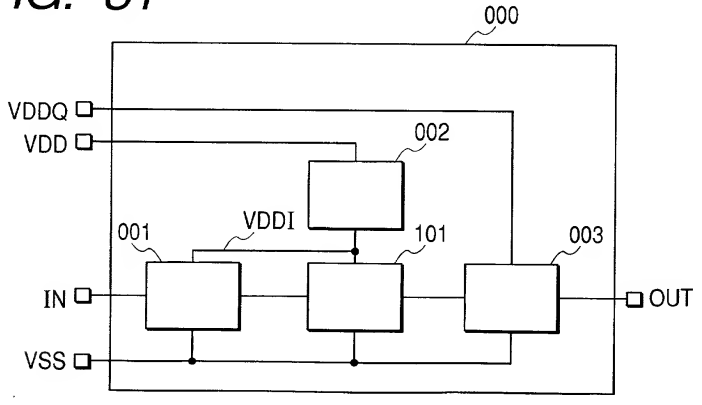


FIG. 32

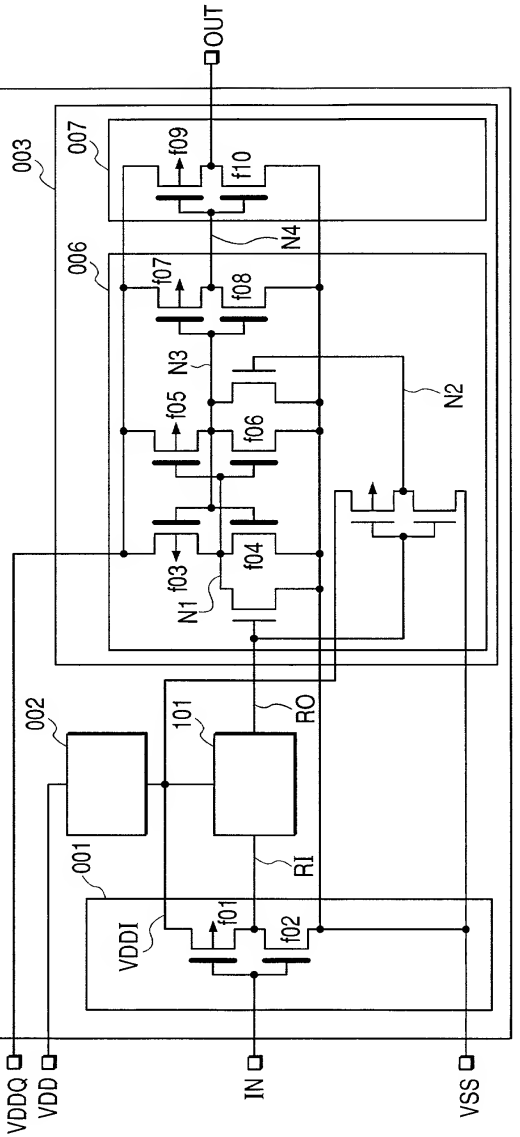

OUT
000
003
007
f09
f10
N4
006
f07
f08
N3
f05
f06
N2
f03
N1
f04
002
101
RO
001
RI
VDDI
f01
f02
VDDQ
VDD
IN
VSS

FIG. 33

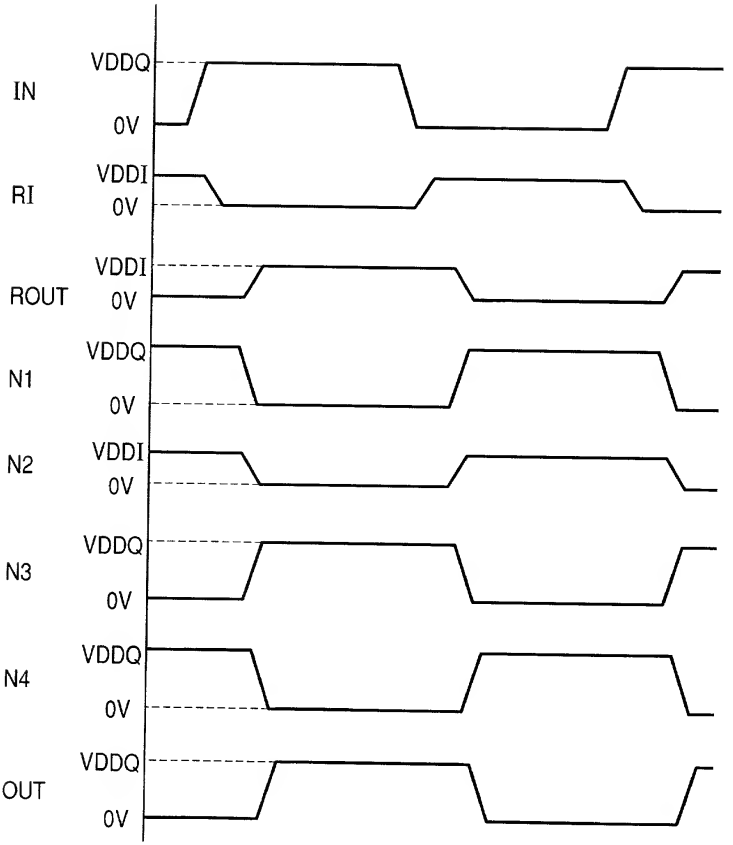
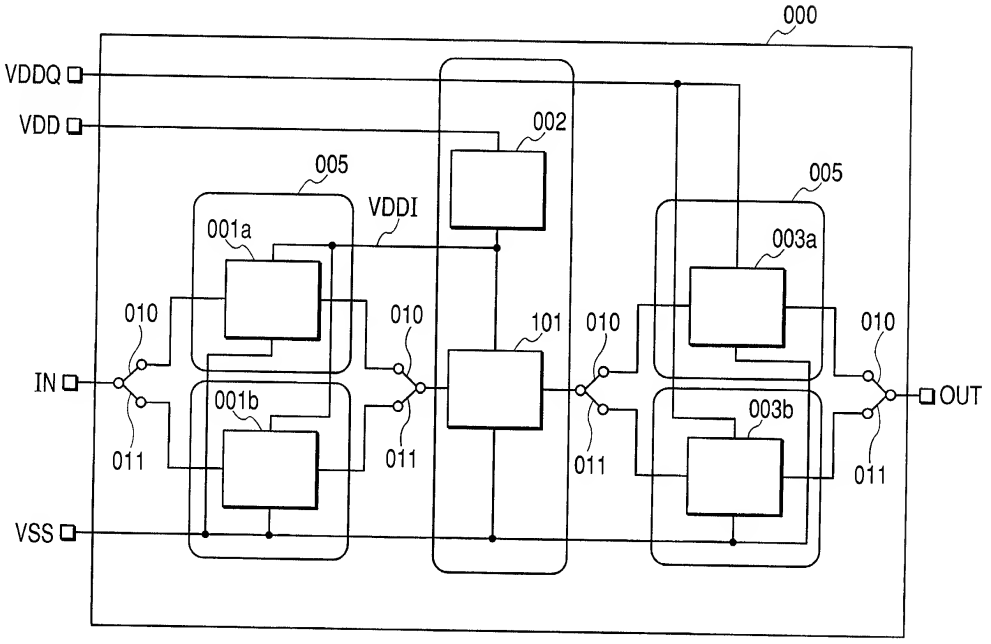

IN
VDDQ
0V
RI
VDDI
0V
ROUT
VDDI
0V
N1
VDDQ
0V
N2
VDDI
0V
N3
VDDQ
0V
N4
VDDQ
0V
OUT
VDDQ
0V

FIG. 34


000
VDDQ
VDD
002
005
VDDI
001a
005
003a
010
010
101
010
010
IN
001b
003b
OUT
011
011
011
011
VSS